I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to : Commissioner of Patents and Trademarks, Washington, D.C. 20231, on October 20, 2003. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

Karen Cinq-Mars 10/20/03
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	October 20, 2003
Geng Wang, et al. :	Group Art Unit:
Serial No. 10/604,731 :	Examiner:
Filed: 8/13/03 :	International Business Machines Corporation 2070 Route 52 Hopewell Junction, NY 12533

TITLE: SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Geng Wang, et al.

By H. Daniel Schnurmann

H. Daniel Schnurmann
Registration No. 35,791
Telephone No. 845-894-2481

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920030209US1	10/604,731
Applicant(s)	
Geng Wang, et al.	
Filing Date	**Group Art Unit**
8/13/03	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		"Vertical Pass Transistor Design For Sub-100nm DRAM Technologies" K. McStay, et al., Proceedings 2002 Symposium on VLSI Technology, Section 18.3, pp 180-181 June 11, 2002

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.